CLAIMS

What is claimed is:

1. A gate electrode formed on a substrate comprising:
an insulative layer formed on a substrate;
a gate layer formed on the insulative layer;
a conductive layer formed on the gate layer;
thick first spacers formed adjacent to opposite sides of the gate layer wherein the thick first spacers are recessed to create a open space between the both the gate layer and the conductive layer and thick second spacers; and,
thick second spacers formed adjacent to each of the thick first spacers.

2. The gate electrode of claim 1 wherein the insulative layer is an oxide.

3. The gate electrode of claim 2 wherein the gate layer is a polysilicon.

4. The gate electrode of claim 3 wherein the conductive layer is a polycide.

5. The gate electrode of claim 4 wherein the thick first spacers are an oxide.

6. The gate electrode of claim 5 wherein the thick second spacers are a nitride.

7. The gate electrode of claim 6 wherein the polycide is titanium salicide ($TiSi_2$).

8. A gate electrode formed on a substrate comprising:
an insulative layer formed on a substrate;
a gate layer formed on the insulative layer;
a conductive layer formed on the gate layer;
thin first spacers formed adjacent to opposite sides of the gate layer wherein the thin first spacers are recessed; and,

thick second spacers formed adjacent to each of the thin first spacers wherein the thick second spacers are recessed.

9. The gate electrode of claim 8 wherein the insulative layer is an oxide.

10. The gate electrode of claim 9 wherein the gate layer is a polysilicon.

11. The gate electrode of claim 10 wherein the conductive layer is a polycide.

12. The gate electrode of claim 11 wherein the thin first spacers are an oxide.

13. The gate electrode of claim 12 wherein the thick second spacers are a nitride.

14. The gate electrode of claim 13 wherein the polycide is titanium salicide ($TiSi_2$).

15. A gate electrode formed on a substrate comprising:
an insulative layer formed on a substrate;
a gate layer formed on the insulative layer;
a conductive layer formed on the gate layer;
thin first spacers formed adjacent to opposite sides of the gate layer; and,
thick second spacers formed adjacent to each of the thin first spacers wherein the thick second spacers are partially recessed to form thin second spacer walls adjacent to the thin first spacers in a region adjacent to the conductive layer.

16. The gate electrode of claim 15 wherein the insulative layer is an oxide.

17. The gate electrode of claim 16 wherein the gate layer is a polysilicon.

18. The gate electrode of claim 17 wherein the conductive layer is a polycide.

19. The gate electrode of claim 18 wherein the thin first spacers are an oxide.

20. The gate electrode of claim 19 wherein the thick second spacers are a nitride.

21. The gate electrode of claim 20 wherein the polycide is titanium salicide ($TiSi_2$).

22. A gate electrode formed on a substrate comprising:

an insulative layer formed on a substrate;

a gate layer formed on the insulative layer;

a conductive layer formed on the gate layer;

thin first spacers formed adjacent to opposite sides of the gate layer;

thin second spacers formed adjacent to each of the thin first spacers;

thin third spacers formed adjacent to each of the thin second spacers wherein the thin third spacers are recessed; and,

thick fourth spacers formed adjacent to each of the thin third spacers wherein the thick fourth spacers are recessed.

23. The gate electrode of claim 22 wherein the insulative layer is an oxide.

24. The gate electrode of claim 23 wherein the gate layer is a polysilicon.

25. The gate electrode of claim 24 wherein the conductive layer is a polycide.

26. The gate electrode of claim 25 wherein the thin first spacers are an oxide.

27. The gate electrode of claim 26 wherein the thin second spacers are a nitride.

28. The gate electrode of claim 27 wherein the thin third spacers are an oxide.

29. The gate electrode of claim 28 wherein the thick fourth spacers are a nitride.

30. The gate electrode of claim 29 wherein the polycide is titanium salicide ($TiSi_2$).

31. A gate electrode formed on a substrate comprising:

an insulative layer formed on a substrate;

a gate layer formed on the insulative layer;

a conductive layer formed on the gate layer;

thin first spacers formed adjacent to opposite sides of the gate layer wherein the thin first spacers are recessed;

thin second spacers formed adjacent to opposite sides of the thin first spacers wherein the thin second spacers are recessed;

thin third spacers formed adjacent to opposite sides of the thin second spacers wherein the thin third spacers are recessed; and,

thick fourth spacers formed adjacent to opposite sides of the thin third spacers wherein the thick fourth spacers are recessed.

32. The gate electrode of claim 31 wherein the insulative layer is an oxide.

33. The gate electrode of claim 32 wherein the gate layer is a polysilicon.

34. The gate electrode of claim 33 wherein the conductive layer is a polycide.

35. The gate electrode of claim 34 wherein the thin first spacers are an oxide.

36. The gate electrode of claim 35 wherein the thin second spacers are a nitride.

37. The gate electrode of claim 36 wherein the thin third spacers are an oxide.

38. The gate electrode of claim 37 wherein the thick fourth spacers are a nitride.

39. The gate electrode of claim 38 wherein the polycide is titanium salicide ($TiSi_2$).

40. A method for forming a gate electrode comprising the steps of:

providing a substrate with an insulative layer deposited thereon;

forming a gate layer on the insulative layer;

depositing a thick first spacer layer on the gate layer and the substrate;

depositing a thick second spacer layer on the thick first spacer layer;

removing a portion of the thick second spacer layer to form thick second spacers adjacent to the thick first spacer layer;

removing a portion of the thick first spacer layer to form recessed thick first spacers adjacent to the gate layer wherein a space is formed between the gate layer and the thick second spacers;

depositing a layer of reactant on the gate layer;

annealing the layer of reactant and the gate layer to form a conductive layer; and,

removing the unreacted reactant layer.

41. The method of claim 40 wherein removing a portion of the thick second spacer layer to form thick second spacers is by anisotropic etching.

42. The method of claim 41 wherein the removing a portion of the thick first spacer layer to form thick first spacers is by isotropic etching.

43. The method of claim 42 wherein the insulative layer is an oxide.

44. The method of claim 43 wherein the gate layer is a polysilicon.

45. The method of claim 44 wherein the reactant is a metal.

46. The method of claim 45 wherein said thick first spacer layer is an oxide.

47. The method of claim 46 wherein said thick second spacer layer is a nitride.

48. The method of claim 47 wherein the conductive layer is a polycide.

49. The method of claim 48 wherein the metal is titanium.

50. The method of claim 49 wherein the polycide is titanium salicide ($TiSi_2$).

51. A method for forming a gate electrode comprising the steps of:
providing a substrate with a gate oxide layer deposited thereon;
forming a gate layer on the insulative layer;
depositing a thin first spacer layer on the gate layer and the substrate;
depositing a thick second spacer layer on the thin first spacer layer;
removing a portion of the thick second spacer layer to form recessed thick second spacers;
removing a portion of the thin first spacer layer to form recessed thin first spacers;
depositing a layer of reactant on the gate layer;
annealing the layer of reactant and the gate layer to form a conductive layer; and,
removing the unreacted reactant layer.

52. The method of claim 51 wherein removing a portion of the thick second spacer layer to form thick second spacers is by anisotropic etching.

53. The method of claim 52 wherein the removing a portion of the thin first spacer layer to form thin first spacers is by isotropic etching.

54. The method of claim 53 wherein the insulative layer is an oxide.

55. The method of claim 54 wherein the gate layer is a polysilicon.

56. The method of claim 55 wherein the reactant is a metal.

57. The method of claim 56 wherein said thin first spacer layer is an oxide.

58. The method of claim 57 wherein said thick second spacer layer is a nitride.

59. The method of claim 58 wherein the conductive layer is a polycide.

60. The method of claim 59 wherein the metal is titanium.

61. The method of claim 60 wherein the polycide is titanium salicide ($TiSi_2$).

62. A method for forming a gate electrode comprising the steps of:

providing a substrate with an insulative layer deposited thereon;

forming a gate layer on the insulative layer;

depositing a thin first spacer layer on the gate layer and the substrate;

depositing a thick second spacer layer on the thin first spacer layer;

removing a portion of the thick second spacer layer to form partially recessed thick second spacers;

removing a portion of the thin first spacer layer to form thin first spacers;

depositing a layer of reactant on the gate layer;

annealing the layer of reactant and the gate layer to form a conductive layer; and,

removing the unreacted reactant layer.

63. The method of claim 62 wherein removing a portion of the thick second spacer layer to form partially recessed thick second spacers further comprises:

removing a first portion of the thick second spacer by anisotropic etching; and,

removing a second portion of the thick second spacer layer by isotropic etching to form thin second spacer walls adjacent to the thin first spacers and in a region adjacent to the conductive layer.

64. The method of claim 63 wherein removing a portion of the thin first spacer layer to form thin first spacers is by anisotropic etching.

65. The method of claim 64 wherein the insulative layer is an oxide.

66. The method of claim 65 wherein the gate layer is a polysilicon.

67. The method of claim 66 wherein the reactant is a metal.

68. The method of claim 67 wherein said thin first spacer layer is an oxide.

69. The method of claim 68 wherein said thick second spacer layer is a nitride.

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70. The method of claim 69 wherein the conductive layer is a polycide.

71. The method of claim 70 wherein the metal is titanium.

72. The method of claim 71 wherein the polycide is titanium salicide ($TiSi_2$).

73. A method for forming a gate electrode comprising the steps of :

providing a substrate with an insulative layer deposited thereon;

forming a gate layer on the insulative layer;

depositing a thin first spacer layer on the gate layer and the substrate;

depositing a thin second spacer layer on the thin first spacer layer;

removing a portion of the thin second spacer layer to form thin second spacers;

removing a portion of the thin first spacer layer to form thin first spacers;

30 depositing a thin third spacer layer;

depositing a thick fourth spacer layer on the thin third spacer layer;

removing a portion of the thick fourth spacer layer to form recessed thick fourth spacers;

removing a portion of the thin third spacer layer to form recessed thin third spacers;

depositing a layer of reactant on the gate layer;

annealing the layer of reactant and the gate layer to form a conductive layer; and,

removing the unreacted reactant layer.

74. The method of claim 73 wherein removing a portion of the thin second spacer layer to form thin second spacers is by anisotropic etching.

75. The method of claim 74 wherein removing a portion of the thin first spacer layer to form thin first spacers is by anisotropic etching.

76. The method of claim 75 wherein removing a portion of the thick fourth spacer layer to form recessed thick fourth spacers further comprises:

removing a first portion of the thick fourth spacer layer by anisotropic etching; and,

removing a second portion of the thick fourth spacer by isotropic etching.

77. The method of claim 76 wherein removing a portion of the thin third spacer layer to form recessed thin third spacers is by anisotropic etching.

78. The method of claim 77 wherein the insulative layer is an oxide.

79. The method of claim 78 wherein the gate layer is a polysilicon.

80. The method of claim 79 wherein the reactant is a metal.

81. The method of claim 80 wherein said thin first spacer layer is an oxide.

82. The method of claim 81 wherein said thin second spacer layer is a nitride.

83. The method of claim 82 wherein said thin third spacer layer is an oxide.

84. The method of claim 83 wherein said thick fourth spacer layer is a nitride.

85. The method of claim 84 wherein the conductive layer is a polycide.

86. The method of claim 85 wherein the metal is titanium.

87. The method of claim 86 wherein the polycide is titanium salicide ($TiSi_2$).

88. A method for forming a gate electrode comprising the steps of :

providing a substrate with an insulative layer deposited thereon;

forming a gate layer on the insulative layer;

depositing a thin first spacer layer on the gate layer and the substrate;

depositing a thin second spacer layer on the thin first spacer layer;

removing a portion of the thin second spacer layer to form thin second spacers;

removing a portion of the thin first spacer layer to form thin first spacers;

depositing a thin third spacer layer;

depositing a thick fourth spacer layer on the thin third spacer layer;

removing a portion of the thick fourth spacer layer to form recessed thick fourth spacers;

removing a portion of the thin third spacer layer to form recessed third spacers;

forming a protective layer on the substrate and gate layer;

removing a portion of the thin second spacers to form recessed thin second spacers;

removing the protective layer and removing a portion of the thin first spacers to form recessed thin first spacers;

depositing a layer of reactant on the gate layer;

annealing the layer of reactant and the gate layer to form a conductive layer; and,

removing the unreacted reactant layer.

89. The method of claim 88 wherein removing a portion of the thin second spacer layer to form thin second spacers is by anisotropic etching.

90. The method of claim 89 wherein removing a portion of the thin first spacer layer to form thin first spacers is by anisotropic etching.

91. The method of claim 90 wherein removing a portion of the thick fourth spacer layer to form recessed thick fourth spacers further comprises:

removing a first portion of the thick fourth spacer layer by anisotropic etching; and,

removing a second portion of the thick fourth spacer layer by isotropic etching.

92. The method of claim 91 wherein removing a portion of the thin third spacer layer to form recessed thin third spacers is by anisotropic etching.

93. The method of claim 92 wherein removing a portion of the thin second spacers to form recessed thin second spacers is by isotropic etching.

94. The method of claim 93 wherein removing the protective layer and removing a portion of the thin first spacers to form recessed thin first spacers is by isotropic etching.

95. The method of claim 94 wherein the insulative layer is an oxide.

96. The method of claim 95 wherein the gate layer is a polysilicon.

97. The method of claim 96 wherein the reactant is a metal.

98. The method of claim 97 wherein the thin first spacer layer is an oxide.

99. The method of claim 98 wherein the thin second spacer layer is a nitride.

100. The method of claim 99 wherein the thin third spacer layer is an oxide.

101. The method of claim 100 wherein the thick fourth spacer layer is a nitride.

102. The method of claim 101 wherein the protective layer is an oxide.

103. The method of claim 101 wherein the conductive layer is a polycide.

104. The method of claim 102 wherein the metal is titanium.

105. The method of claim 103 wherein the polycide is titanium salicide ($TiSi_2$).

106. A method for forming a gate electrode comprising the steps of :

providing a substrate with an insulative layer deposited thereon;

forming a gate layer on the insulative layer;

depositing a thin first spacer layer on the gate layer and the substrate;

depositing a thin second spacer layer on the thin first spacer layer;

removing a portion of the thin second spacer layer to form thin second spacers;

removing a portion of the thin first spacer layer to form thin first spacers;

depositing a thin third spacer layer;

depositing a thick fourth spacer layer on the thin third spacer layer;

removing a portion of the thick fourth spacer layer to form recessed thick fourth spacers;

removing a portion of the thin third spacer layer to form recessed third spacers;

removing a portion of the thin second spacers to form recessed thin second spacers;

removing a portion of the thin first spacers to form recessed thin first spacers;

depositing a layer of reactant on the gate layer;

annealing the layer of reactant and the gate layer to form a conductive layer; and,

removing the unreacted reactant layer.

107. The method of claim 105 wherein removing a portion of the thin second spacer layer to form thin second spacers is by anisotropic etching.

108. The method of claim 106 wherein removing a portion of the thin first spacer layer to form thin first spacers is by anisotropic etching.

109. The method of claim 107 wherein removing a portion of the thick fourth spacer layer to form recessed thick fourth spacers further comprises:

removing a first portion of the thick fourth spacer layer by anisotropic etching; and,

15 removing a second portion of the thick fourth spacer layer by isotropic etching.

110. The method of claim 108 wherein removing a portion of the thin third spacer layer to form recessed thin third spacers is by anisotropic etching.

111. The method of claim 109 wherein removing a portion of the thin second spacers to form recessed thin second spacers is by isotropic etching.

112. The method of claim 110 wherein removing a portion of the thin first spacers to form recessed thin first spacers is by isotropic etching.

113. The method of claim 111 wherein the insulative layer is an oxide.

114. The method of claim 112 wherein the gate layer is a polysilicon.

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115. The method of claim 113 wherein the reactant is a metal.

116. The method of claim 114 wherein the thin first spacer layer is an oxide.

117. The method of claim 115 wherein the thin second spacer layer is a nitride.

118. The method of claim 116 wherein the thin third spacer layer is an oxide.

119. The method of claim 117 wherein the thick fourth spacer layer is a nitride.

120. The method of claim 118 wherein the conductive layer is a polycide.

121. The method of claim 119 wherein the metal is titanium.

122. The method of claim 120 wherein the polycide is titanium salicide ($TiSi_2$).

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